Intel's 90 nm Process Starting High Volume Manufacturing

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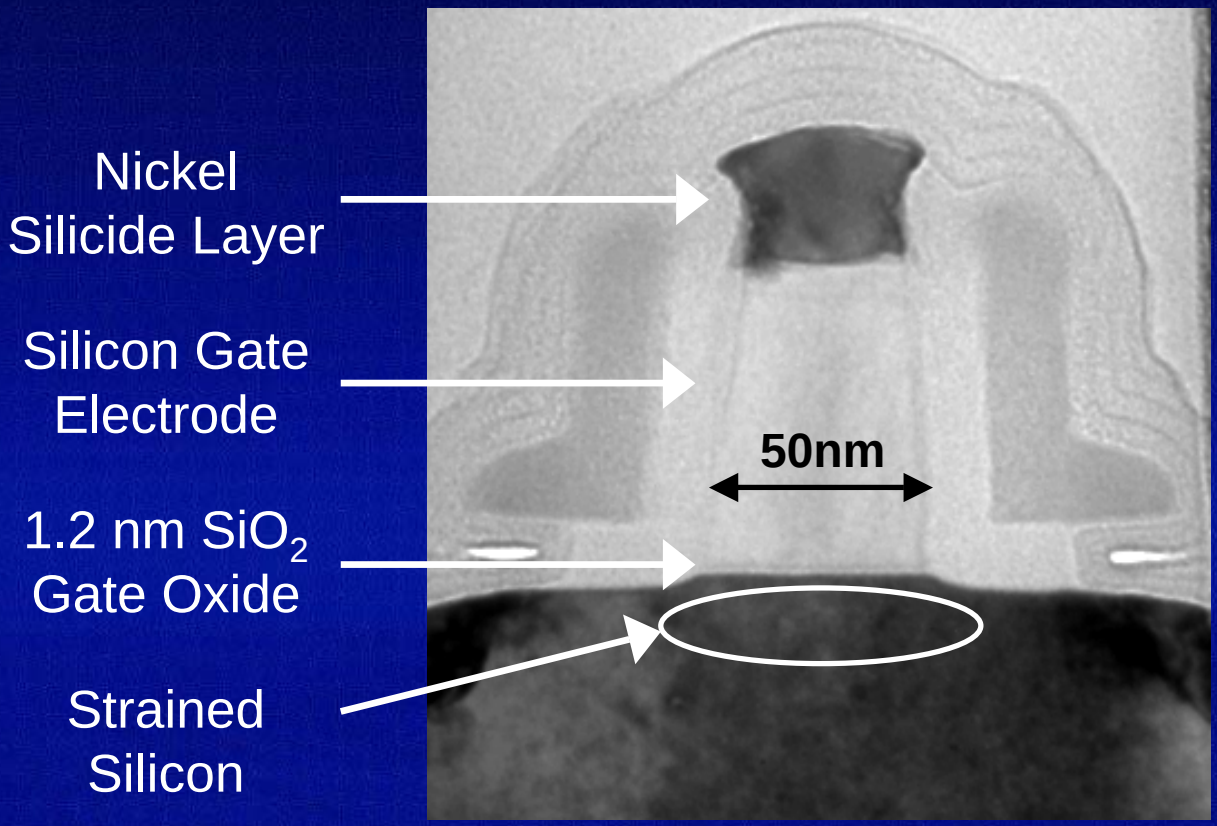
A New Process Every 2 Years

Process Name	P854	P856	P858	Px60	P1262	P1264
1st Production	1995	1997	1999	2001	2003	2005
Lithography	0.35μm	0.25μm	0.18μm	0.13μm	90nm	65nm
Gate Length	0.35μm	0.20μm	0.13μm	<70nm	<50nm	<35nm
Wafer (mm)	200	200	200	200/300	300	300

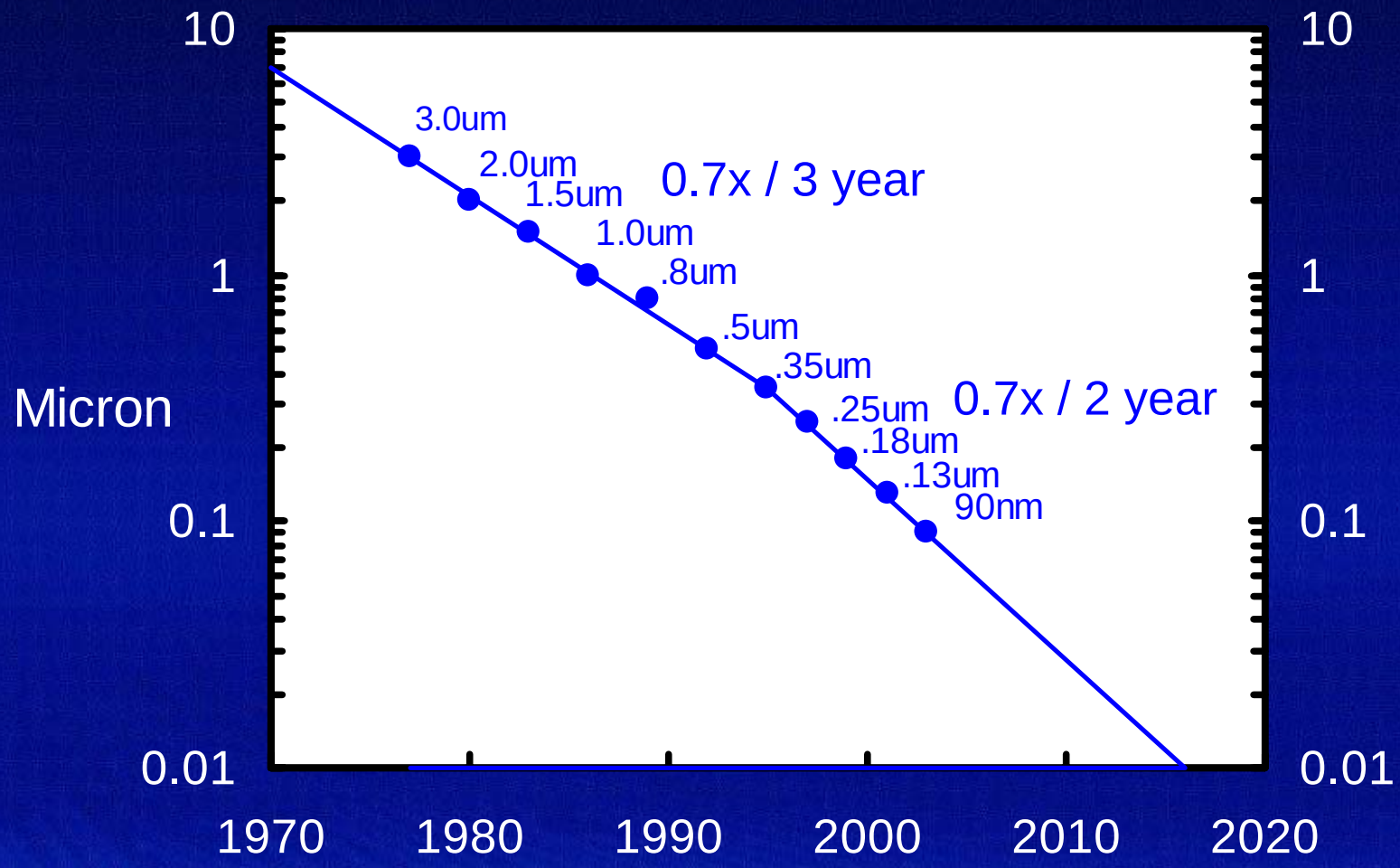
Moore's Law continues!

90 nm Generation Transistor



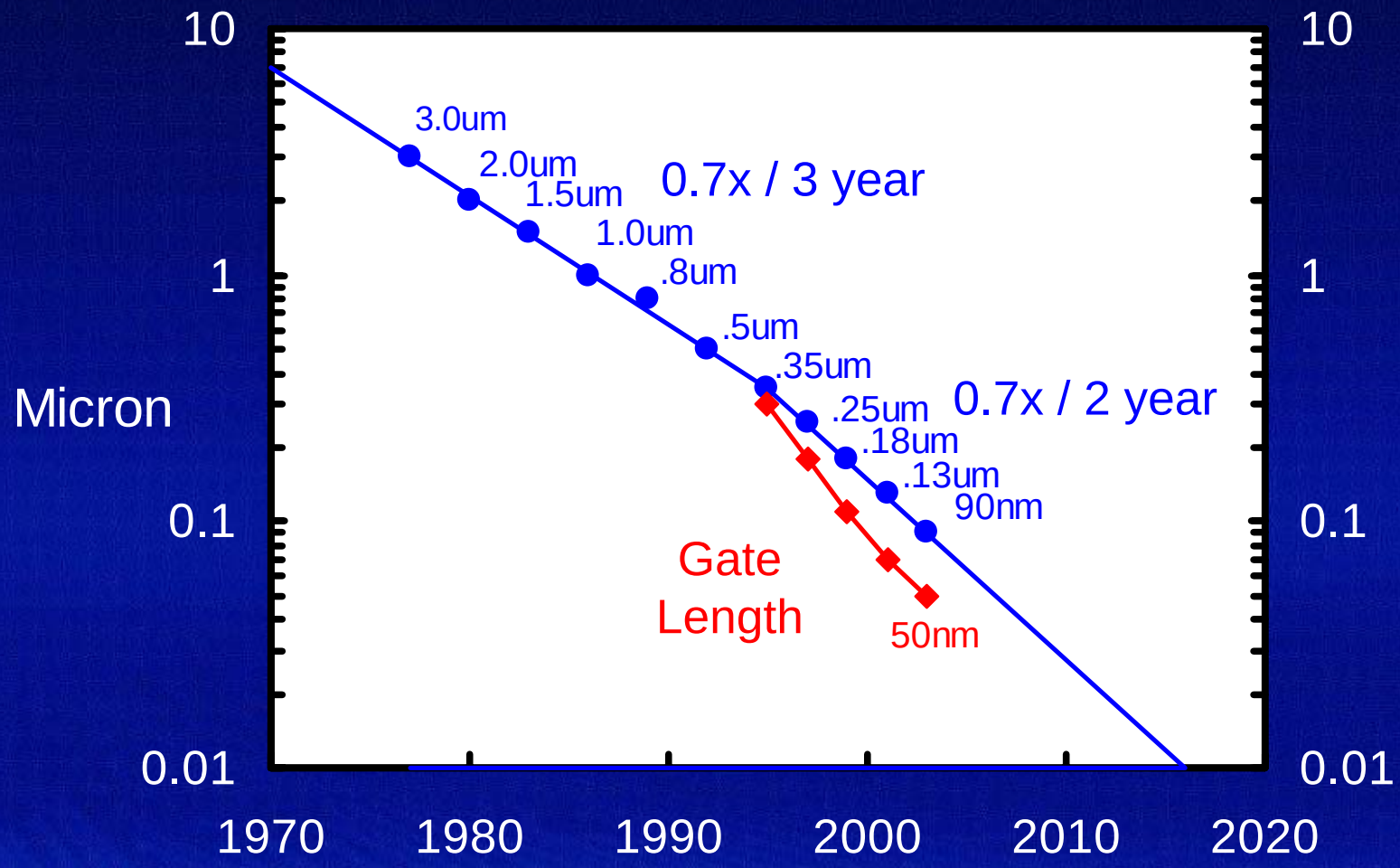
No other company combines these transistor features at the 90 nm generation

Typical Feature Size Scaling



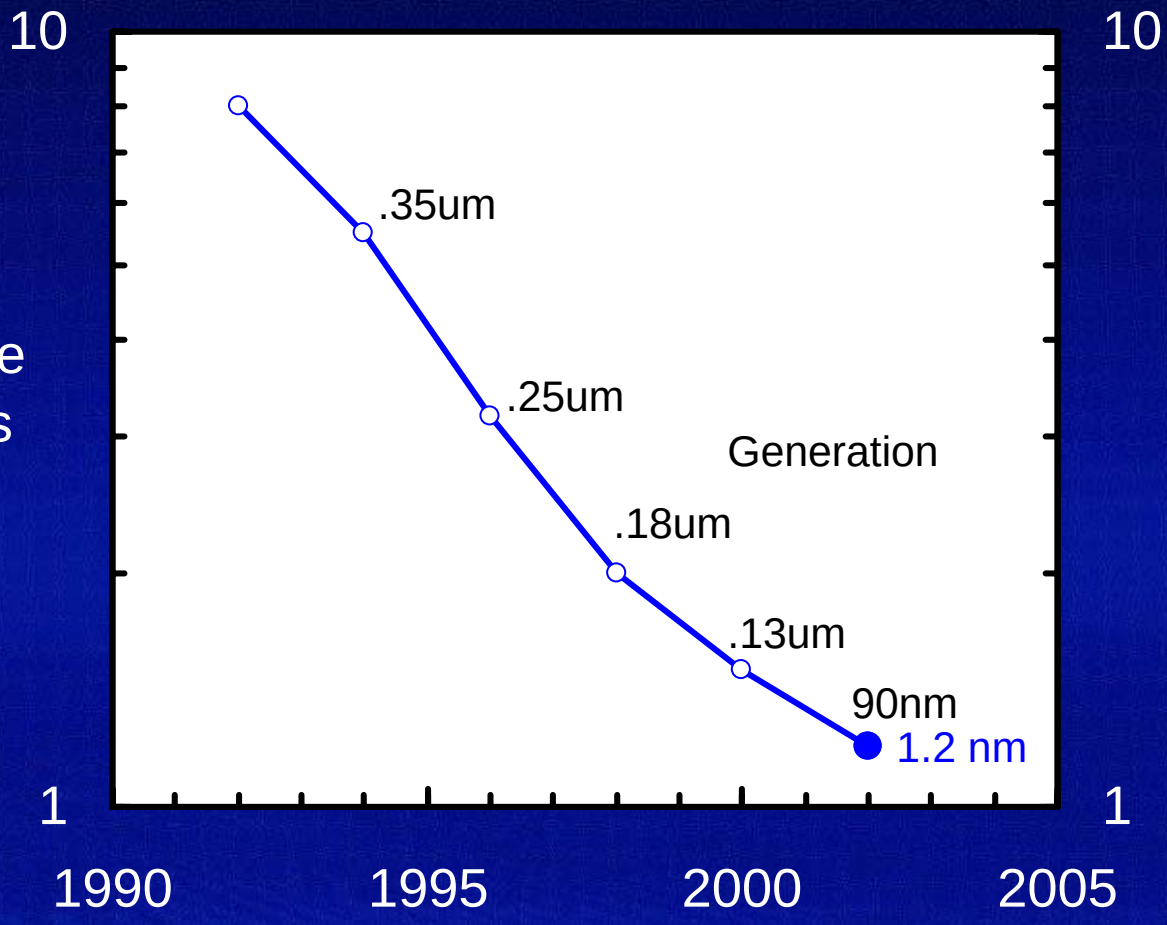
Feature size scaling has accelerated

Transistor Gate Length Scaling



Faster gate length scaling to maintain transistor performance lead

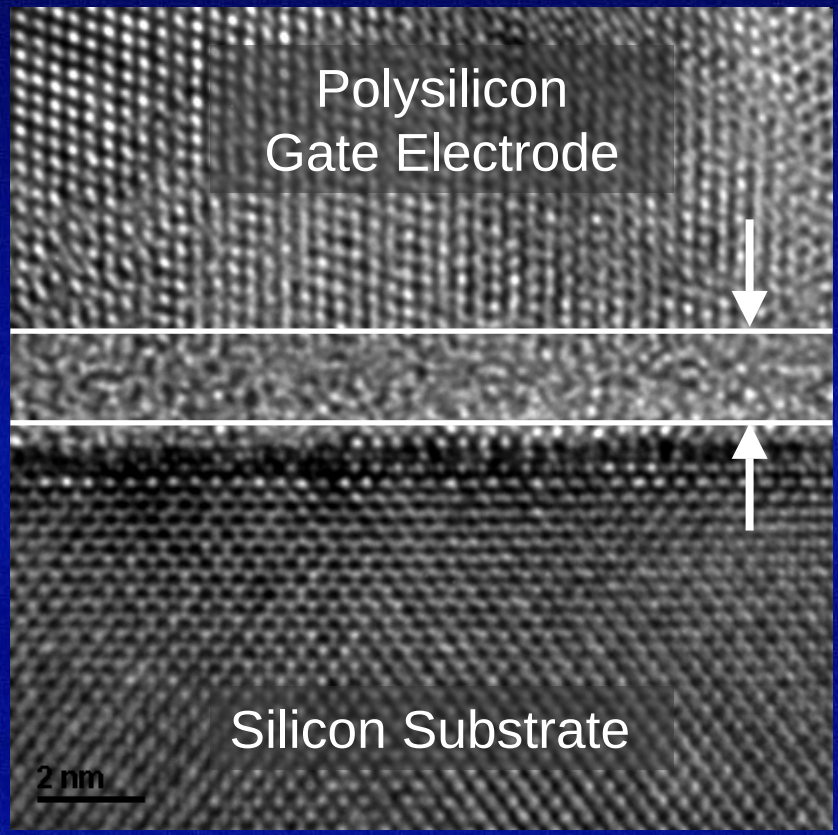
Gate Oxide Scaling



Intel leads the industry in gate oxide scaling

Thinner gate oxide increases transistor performance

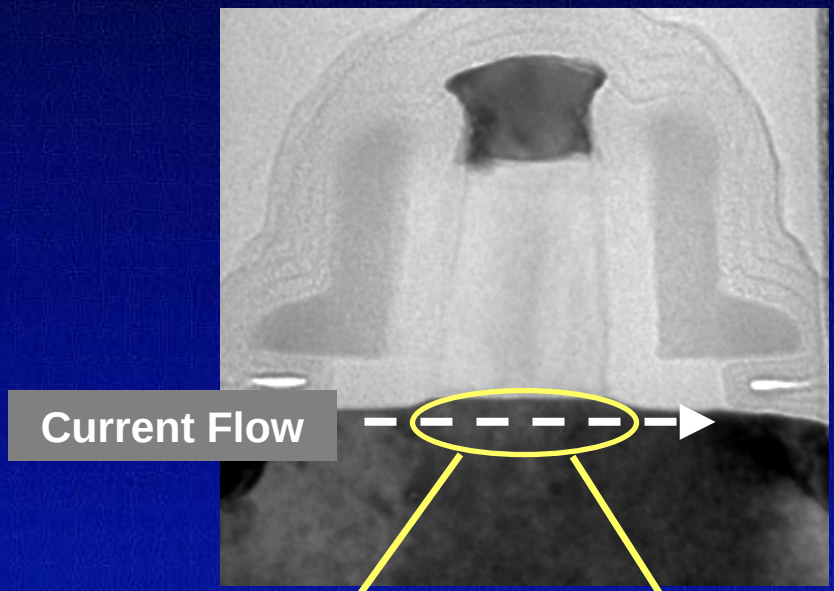
90 nm Generation Gate Oxide



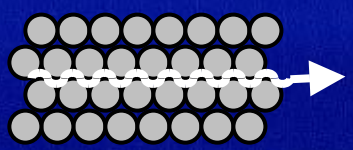
1.2 nm SiO_2

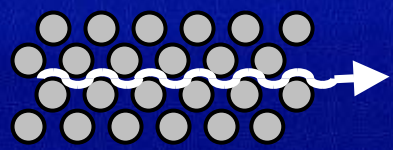
Gate oxide is less than 5 atomic layers thick

Strained Silicon Transistors



Normal electron flow





Faster electron flow

Normal Silicon Lattice

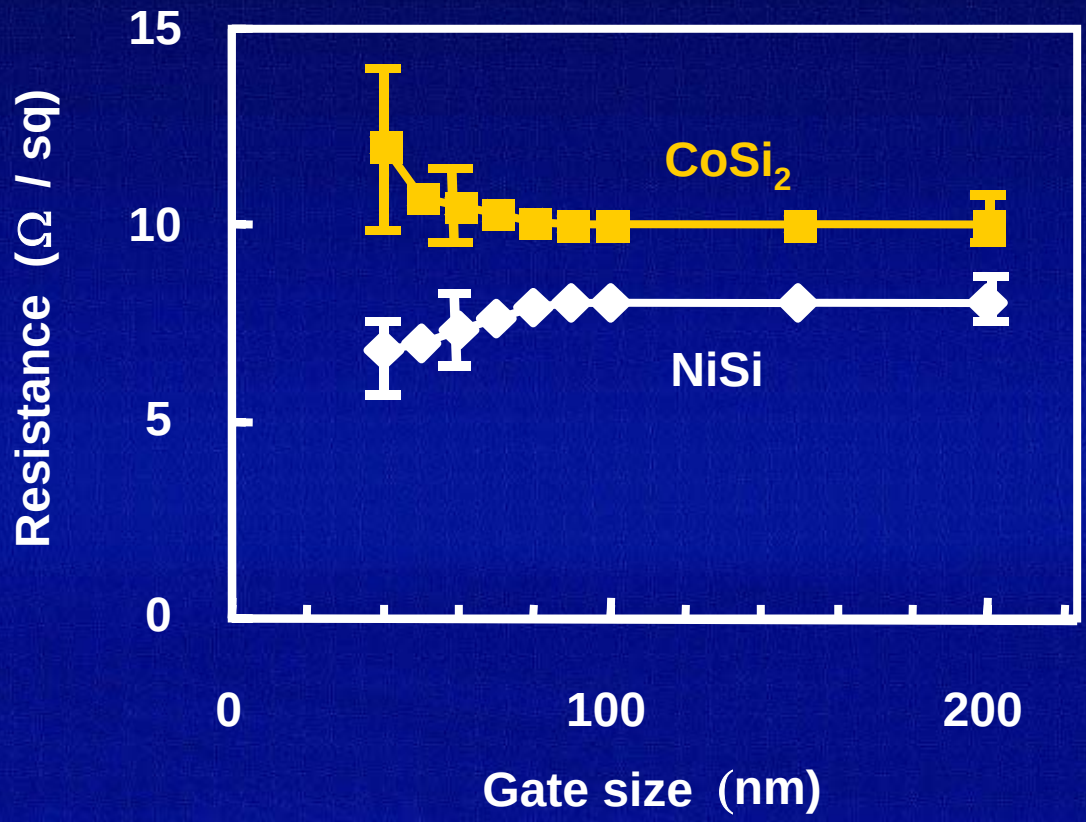
Strained Silicon Lattice

Strained silicon provides 10-20% transistor drive current boost

10-20% is ~half generation transistor performance gain

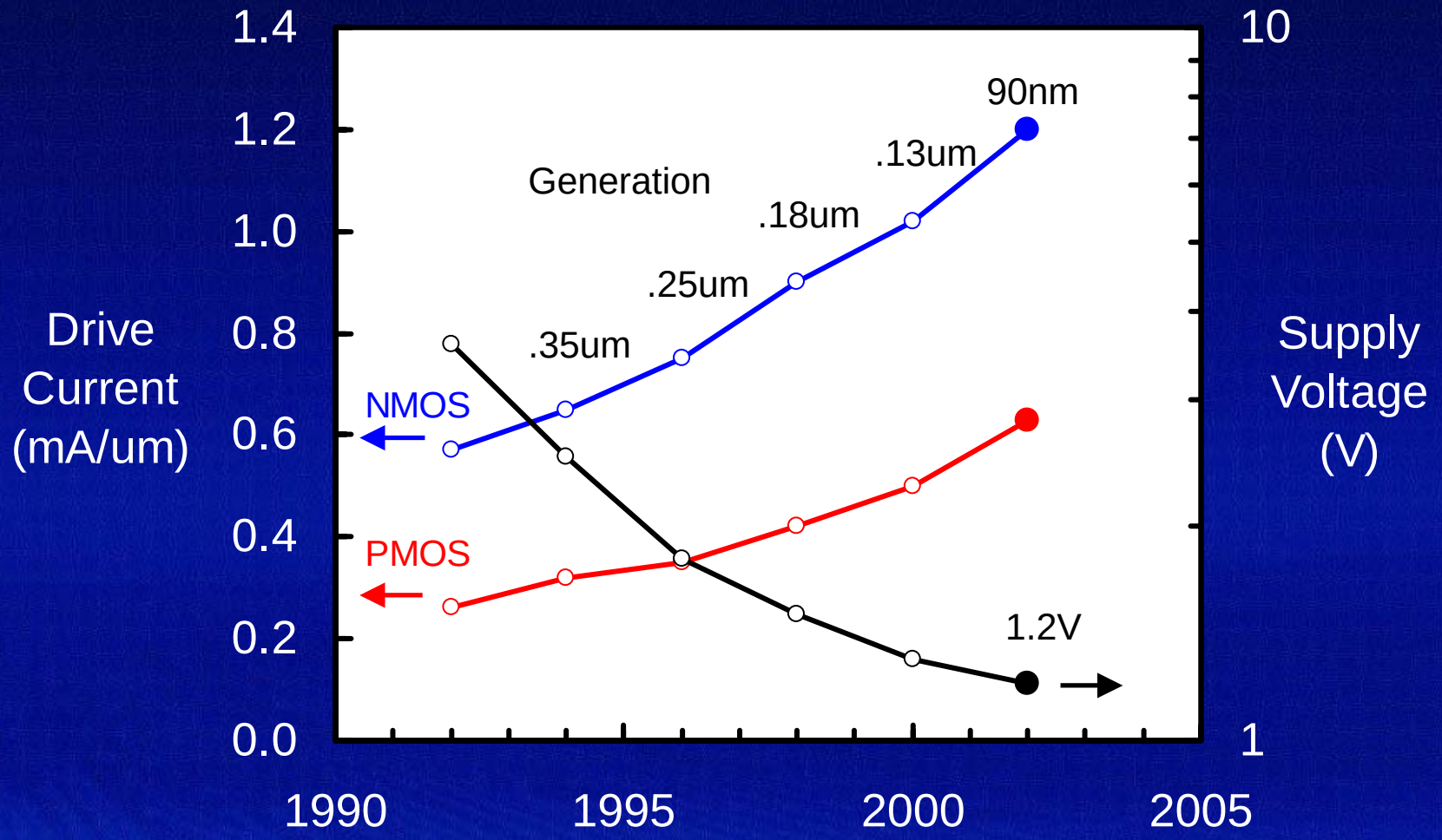
Intel is ramping 90 nm CPU products using strained silicon

NiSi for Low Gate Resistance



Nickel silicide provides lower line resistance for sub-100 nm gate lengths

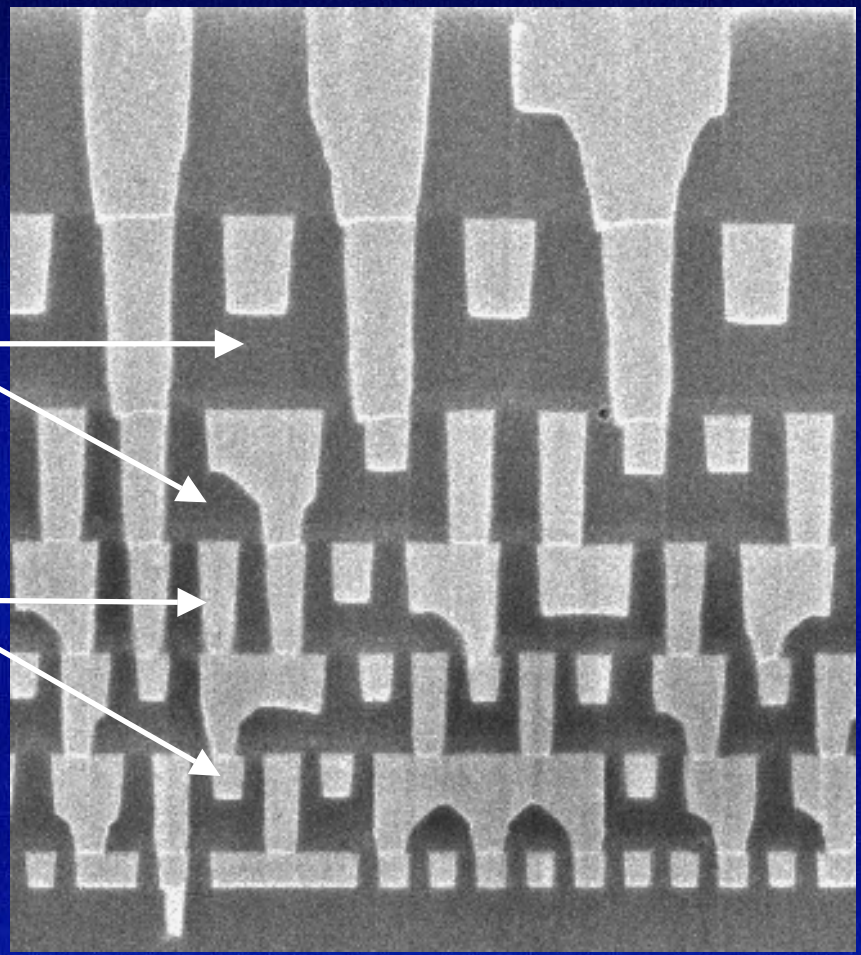
Transistor Performance



Highest drive current in the industry

Reduced supply voltage for lower power

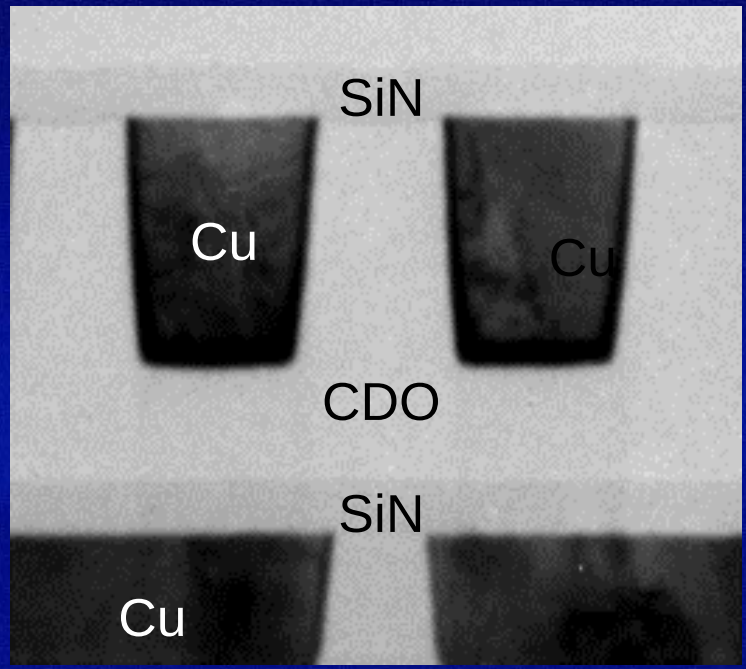
90 nm Generation Interconnects



7 layers of copper + new low-k CDO dielectric

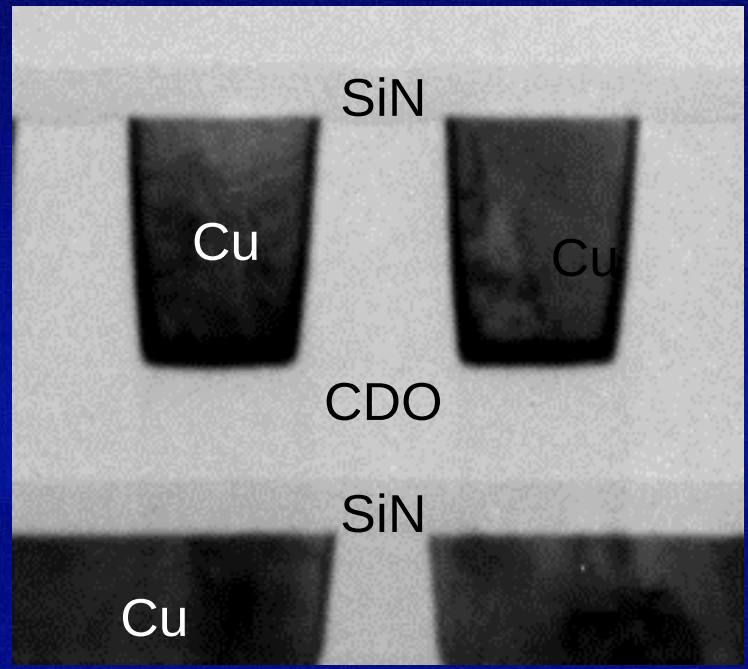
Low-k Carbon Doped Oxide

- New low-k CDO material used for interconnect dielectric
- Low-k CDO provides ~20% capacitance reduction over previous generation
- Lower interconnect capacitance results in faster interconnects
- Process integration and package assembly issues with this new material have been solved

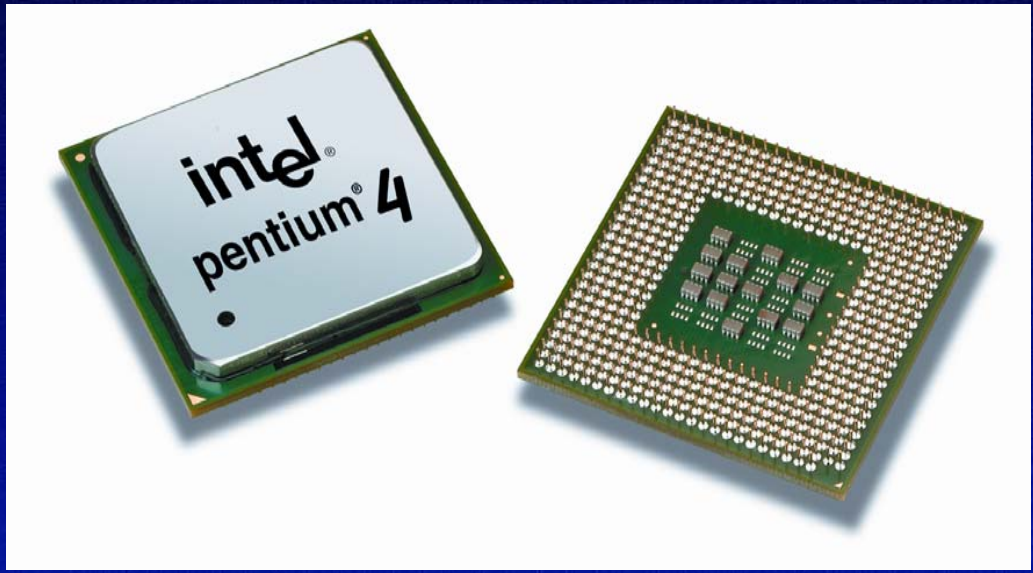


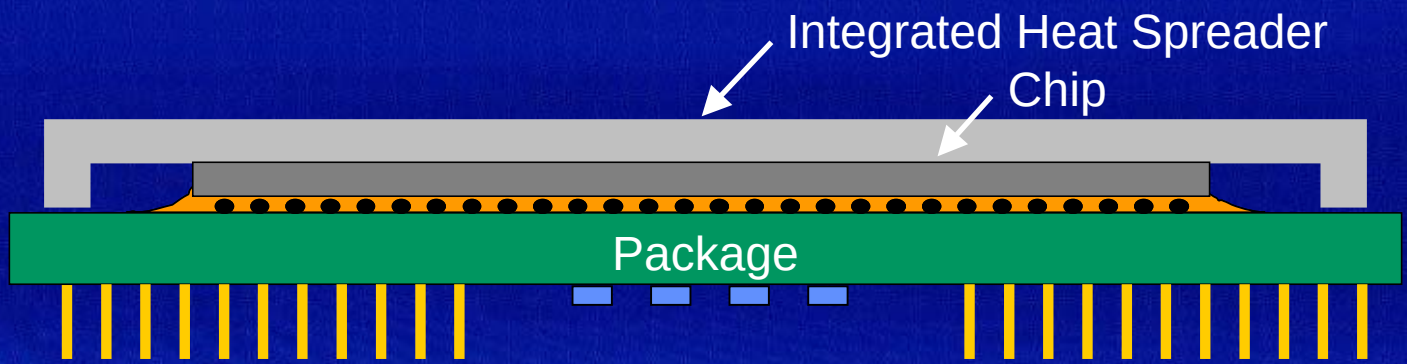
2-Layer Interconnect Dielectric Stack

- Intel uses a simple 2-layer dielectric stack:
  - Low-k CDO dielectric
  - SiN etch stop
- Many of our competitors use a more complex 4-layer stack:
  - Dielectric
  - Etch stop
  - Dielectric
  - Etch stop
- Intel's simpler stack is less costly and reduces capacitance by not having extra etch stop layer



Package Technology



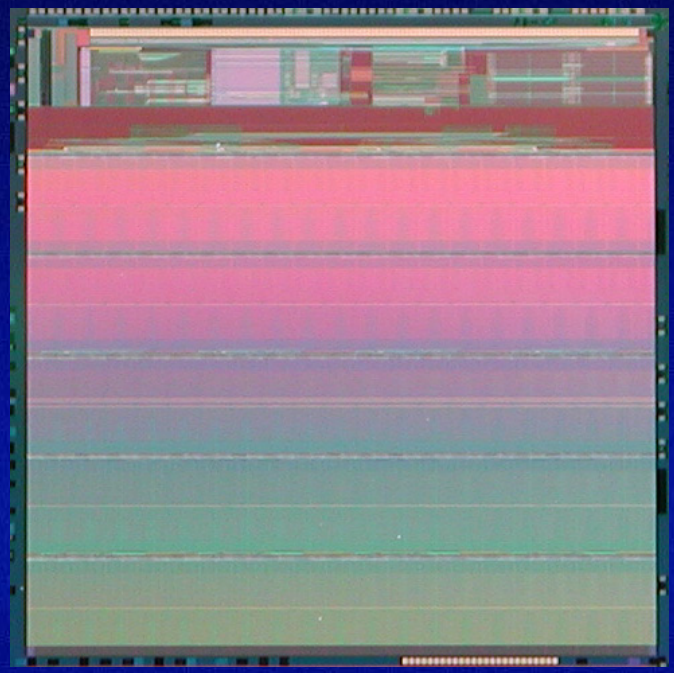


Organic flip-chip packages provide low cost and high performance

1.0 μm^2 SRAM Cell

- Ultra-small SRAM cell packs six transistors in an area of 1.0 μm^2
- Intel was first in the industry to reach this cell size milestone
- Small memory cell enables cost effective increase in CPU performance by adding more on-die cache memory

52 Mbit SRAM Chip



109 mm^2 die size

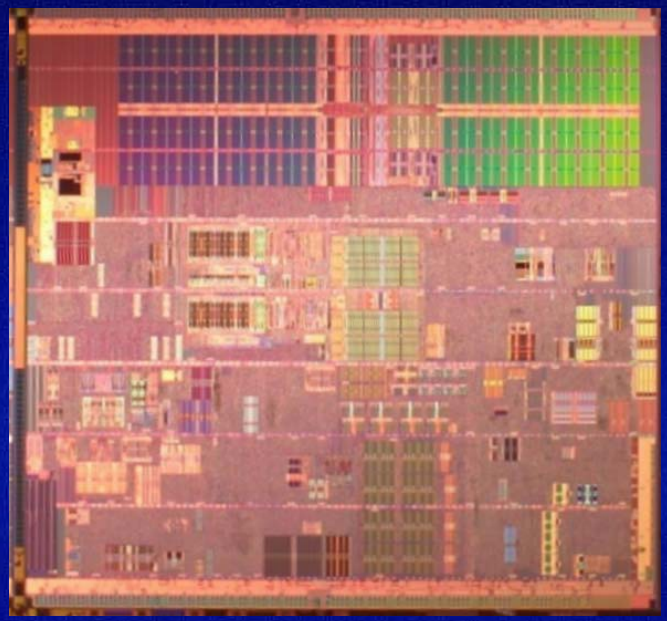
330 million transistors

First silicon: Q1 2002

SRAM chip used to develop/debug 90 nm process

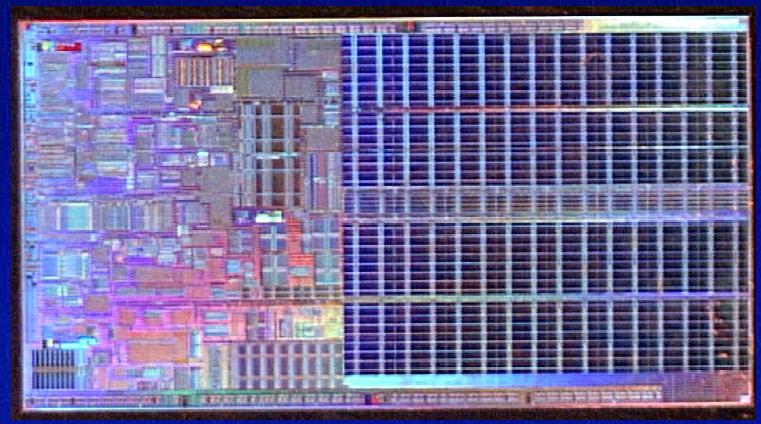
90 nm CPU Chips

Prescott CPU



112 mm^2 die size
125 million transistors

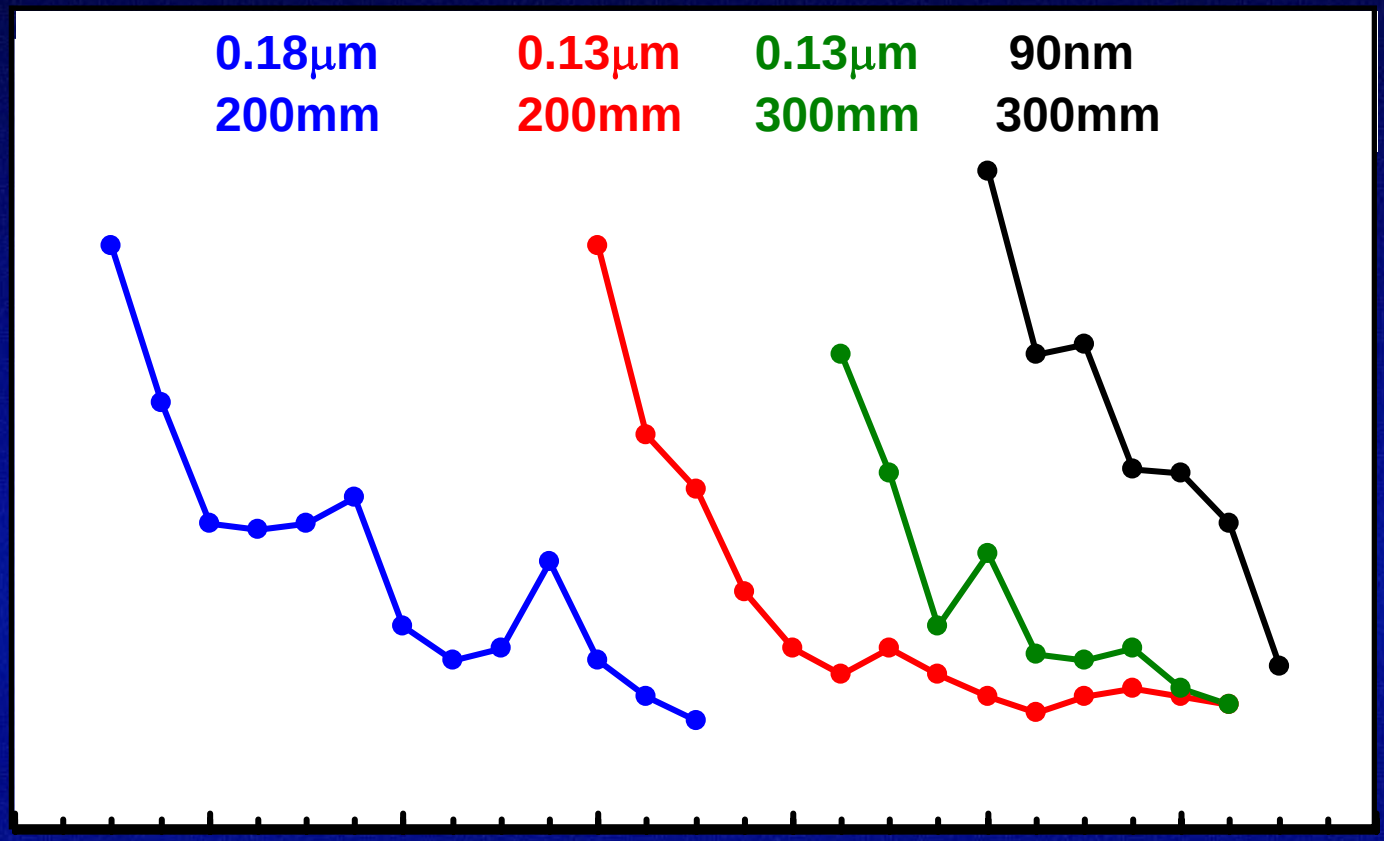
Dothan CPU



87 mm^2 die size
144 million transistors

90 nm process now ramping on high performance CPU products

Yield Trend



90 nm defect reduction trend has been fastest ever

90 nm yields are now at level needed for HVM

Summary

- Intel's 90 nm process incorporates industry-leading transistor features and will be the first to use strained silicon technology in volume manufacturing
- High density, high performance interconnects are provided with 7 layers of copper combined with a new low-k CDO dielectric and organic flip-chip packages
- Advanced CPU products are being ramped on this technology
- 90 nm defect reduction has been fastest ever and yields are now at level needed for high volume manufacturing

For further information on Intel's silicon technology, please visit the Silicon Showcase at www.intel.com/research/silicon